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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/518,642	03/15/2005	Mitsuhiro Yuasa	101249.55749US	2849

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EXAMINER	
EFTEKHARZADEH, ARDESHIR	

ART UNIT	PAPER NUMBER
2815	

NOTIFICATION DATE	DELIVERY MODE
07/09/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Office Action Summary	Application No.	Applicant(s)	
	10/518,642	YUASA, MITSUHIRO	
	Examiner	Art Unit	
	ARDESHIR EFTEKHARZADEH	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *10 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 12-23* is/are pending in the application.

4a) Of the above claim(s) *3,12-15 and 17-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED OFFICE ACTION

Applicant's Amendments

(1) Applicant's amendment to the listing of claims entered on 06/10/2008 is hereby acknowledged. Claims 1-7 and 12-23 are pending, from which claims 3, 12-15 and 17-23 are withdrawn (claims 8-11 are canceled). Claims 1-2 and 4-7 are considered for prosecution merit.

Claim Objections – Minor Informalities

(2) **Claim 1** is objected to for having the following minor informality: "at least one of said switches are connected on each side …." Appropriate correction is required.

Claim Rejections - 35 U.S.C. § 112

(3) The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 112,

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

(4) **Claim 1** is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter Applicant regards as the invention. Claim 1 recites that "switches for connecting each of said circuit elements." It is not clear what the switches are connecting the said circuit elements to. Also claim 1 contains the recitation "at least one of said switches are connected on each side of said circuit elements." It is not clear what the Applicants mean, when they said switches are connected on each side. It is not particularly pointed out or distinctly claimed what constitutes "a side" of an element. It could be a physical side like a side of cube, or it can be geometrically to one side. it is not clear what the applicants regard as their invention. More over the above recitation is vague and indefinite on the additional ground that it does not particularly point out nor does it distinctly claim what the Applicants regard as "connecting." A connection is made between two points that are connected to each other and here it is not clear which two points or two objects are connected to each other.

Claim Rejections - 35 USC § 102

(5) The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(6) **Claims 1 and 2** are rejected under 35 U.S.C. 102(b) as being anticipated by Wallace et al. (US Patent 6,271,728) (hereinafter Wallace).

(7) **Regarding claims 1 and 2**, figure 11 of Wallace discloses a device array comprising: various types of elements (elements such as capacitors and resistors provided in low- and high-pass filters; col. 8, lines 13 – col. 10, line 7) including a plurality of circuit elements of each type and switches (semiconductor transistors T1, T2, T3, etc. as seen in fig. 11; col. 8, line 55-col. 10, line 7). The claim recites the limitation "switches for connecting each of said circuit elements" is firstly vague and indefinite (see paragraph (4)) and secondly is an expression of intended use of switches and not limiting. The limitation recitation "at least one of said switches are connected on each side of said circuit elements" is considered and determined to be, firstly broad as to the recitation of "each side" and secondly vague and indefinite (see paragraph (4)) and thirdly met by the disclosure of Wallace (see for example, Fig. 11). Some of said elements are interconnected by determining an open or close of all of said switches so as to make a circuit (fig. 11 shows a phase shifter circuit composed of four stages, and the biasing of the access transistors, or switches, determines how an input signal will be finally filtered based on what the final circuit connected by the open and closed switches comprises).

(8) The recitation "for producing MEMS device" is merely a recitation of intended use of the circuit detailed in the previous paragraph and does not distinguish the cited prior art from the claimed invention.

(9) **Claims 4 – 11 and 16 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Wallace, in view of Lucas et al. (US 6,287,951 B1)**.

(10) **Regarding claim 4**, Wallace discloses that the device is a fully integrated chipset (col. 3, lines 39-55). It follows that the device will have a semiconductor substrate for the formation of transistors and a conductive interconnect layer to interconnect devices. These limitations are inherent to all integrated semiconductor devices. If Applicant can show that this limitation is not inherent to every integrated semiconductor device, then it would at least been obvious to have a semiconductor substrate and a conductive interconnect layer in order to form a fully integrated device using know techniques. Lucas teaches the use of a device comprising an integrated circuit comprising transistors formed in the substrate (also in the first interconnect level as seen in figure) along with a plurality of elements formed in an interconnect layer (the interconnects are at least resistors). It would have been obvious to modify Wallace with the teachings of Lucas to create a fully integrated device leading to reduced manufacturing costs and reduced size. The recitation "for producing MEMS device" is merely a recitation of intended use of the circuit detailed in the previous paragraph and does not distinguish the cited prior art from the claimed invention.

(11) **Further for claim 4**, Wallace does not explicitly state that the circuit as seen in fig. 11 has the elements formed in an interconnect layer. It would have been obvious, if not inherent to form the elements in an interconnect layer for the purpose of integrating the device. Also, because the gate stacks of the switches reside in the interconnect level with level contacts the switches, the switches themselves are considered to be provided in the interconnect layer due to this proximity.

(12) **Regarding claim 5**, Wallace discloses that all necessary parts are integrated into the chipset (col. 3, lines 39-55) and that the drive parts are to be provided (col. 8, lines 9-12). The recitation "for producing MEMS device" is merely a recitation of intended use of the circuit detailed in the previous paragraph and does not distinguish the cited prior art from the claimed invention.

(13) **Regarding claim 6**, Wallace discloses that the device is capable of filtering an input wave (col. 8, lines 13-24). The recitation "for producing MEMS device" is merely a recitation of intended use of the circuit detailed in the previous paragraph and does not distinguish the cited prior art from the claimed invention.

(14) **Regarding claim 7**, all semiconductor circuits have three-dimensional structures, as they exist in three-dimensions. The recitation "for producing MEMS device" is merely a recitation of intended use of the circuit detailed in the previous paragraph and does not distinguish the cited prior art from the claimed invention.

(15) **Regarding claim 16**, all the devices reside in the same package as all the devices are integrated into the same chipset (col. 3, lines 39-55). The recitation "for producing MEMS device" is merely a recitation of intended use of the circuit detailed in the previous paragraph and does not distinguish the cited prior art from the claimed invention.

Response to Applicant's arguments

(16) Applicants' arguments are considered and found not to be persuasive. Particularly the limitation that "at least one of said switches are connected on each side of said circuit elements" has been found to be disclosed in the cited prior art. Since a "circuit element" has been determined to be a broad limitation, "each side of said circuit element" is also a broad limitation and is met by the cited prior art (see above).

Conclusion

(17) A shortened statutory period for reply to this Office Action is set to expire **THREE MONTH** from the mailing date of this Office Action. Applicant is reminded of the extension of time policy as set forth in 37 CFR § 1.136(a).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ardeshir Eftekharzadeh whose telephone number is (571) 270-3262. The examiner can normally be reached on Monday-Thursday 10:30 AM-9:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for

unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://portal.uspto.gov/external/portal/pair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. E./

Examiner, Art Unit 2815

/Kenneth A Parker/

Supervisory Patent Examiner, Art Unit 2815